

**TITLE OF THE INVENTION**

REDUCED MASK COUNT BURIED LAYER PROCESS

**CROSS-REFERENCE TO RELATED APPLICATIONS**

Related to a corresponding application entitled A Semiconductor Device Manufacturing with a Reduced Mask Count Buried Layer.

**BACKGROUND OF THE INVENTION**

**FIELD OF THE INVENTION**

This invention relates to semiconductor devices and its manufacturing method, and, more specifically, to the formation of buried layers in such devices.

**DESCRIPTION OF RELATED ART**

It is well known in semiconductor processing that the minimization of the number of masking operations in fabricating a semiconductor device is a constant goal. Thus processes which can eliminate a masking operation are highly desirable in the semiconductor processing art.

Fabrication of complementary vertical bipolar devices for analog signal processing on a single integrated circuit with N type and P type buried layers are known in the art. For example, Rupit Patel et al, "a 30V Complementary Bipolar Technology on SOI for High Speed Precision Analog Circuits," IEEE BCTM, pp. 48-50, 1997, and M. C. Wilson et al, "Process HJ: A 30 GHz NPN and 20 GHz PNP Complementary Bipolar Process for High Linearity RF Circuits," IEEE BCTM, pp. 164-167, 1998, describe examples of these types of circuits. In both publications the circuits taught use both N type and P type buried layers which are formed using separate mask and

implant steps to form each buried layer. This requires two masks and two implants to form the two buried layers.

#### **BRIEF SUMMARY OF THE INVENTION**

It is therefore an object of this invention to provide a semiconductor processing method which provides a non selective N buried layer without requiring a masking operation, together with a selective P type buried layer which is formed using a mask. It is also an object of this invention to provide a semiconductor device with a non selective N type buried layer and a selective P type buried layer.

According to the invention, there is provided a semiconductor process wherein a non selective N type buried layer and a selective P type buried layer are formed on a semiconductor device, the dopant used as the N type buried layer dopant having a lower diffusion coefficient than the dopant used as the P type buried layer dopant.

According to the invention, there is further provided a semiconductor device having a non selective N type buried layer and a selective P type buried layer formed on a semiconductor device, the N type majority dopant present in the N type buried layer dopant having a lower diffusion coefficient than the P type majority dopant present in the P type buried layer dopant.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

The aforementioned and other features, characteristics, advantages, and the invention in general will be better understood from the following more detailed description taken in conjunction with the accompanying drawings, in which:

FIGs. 1a-1f are diagrammatical fragmentary cross sections of a portion of a structure used in the fabrication of an integrated circuit which depict a dual N<sup>+</sup> and P<sup>+</sup> buried layer structure with a non selective N<sup>+</sup> buried layer utilizing both vertical and lateral dielectric insulation;

FIG. 2 is a alternate embodiment of FIG. 1e;

FIGs. 3a-3d illustrate an alternate process of forming the N<sup>+</sup> buried layer of FIG. 1b;

FIGs. 4a-4k are diagrammatical fragmentary cross sections of a portion of a structure used in the fabrication of an integrated circuit which depict a dual N<sup>+</sup> and P<sup>+</sup> buried layer structure with a non selective N<sup>+</sup> buried layer utilizing vertical junction insulation and lateral dielectric insulation;

FIGs. 5a-5g are diagrammatical fragmentary cross sections of a portion of a structure used in the fabrication of an integrated circuit which depict a dual N<sup>+</sup> and P<sup>+</sup> buried layer bonded wafer structure with a non selective N<sup>+</sup> buried layer in which the buried layers are formed in a surface of the device wafer that become the bottoms of the final device islands;

FIGs. 6a-6e illustrate an alternate process to that depicted in FIGs. 5a-5e; and

FIGs. 7a-7c are diagrammatical fragmentary cross sections of a portion of a structure used in the fabrication

of an integrated circuit which depict a dual N+ and P+ buried layer single poly dielectric isolation structure with a non selective N+ buried layer in which the buried layers are formed in a surface of the device wafer that become the bottoms of the final device islands.

It will be appreciated that for purposes of clarity and where deemed appropriate, reference numerals have been repeated in the figures to indicate corresponding features, and that the various elements in the drawings have not necessarily been drawn to scale in order to better show the features of the invention.

#### **DETAILED DESCRIPTION OF THE INVENTION**

Turning now to the drawings, all of which are diagrammatical fragmentary cross sections of a portion of a structure used in the fabrication of an integrated circuit, FIGs. 1a-1f depict a dual N+ and P+ buried layer structure with a non selective N+ buried layer utilizing both vertical and lateral dielectric insulation.

As used herein the term "buried layer" refers to a conductive region in a silicon wafer as that term is known in the art for a completed device, and also, during processing of the device, to certain regions which may be located on the surface and elsewhere in a wafer which will become buried layers in a completed device.

FIG. 1a depicts a portion 10 having a silicon carrier or handle wafer 12, an insulator in the form of a bond oxide 14, an silicon-over-insulator (SOI) layer 16 and a surface layer 18 of N type dopants implanted on the entire top surface of the SOI layer 16 as depicted by the arrows at the top of FIG. 1a. The N type dopant implanted in the surface

layer 18 is preferably, but not necessarily, arsenic (As) or antimony (Sb), and, in one preferred embodiment, Sb is implanted at an integrated dose of  $3.75 \times 10^{14}$  atoms/cm<sup>2</sup>.

FIG. 1b is FIG. 1a after several process steps including a diffusion operation which causes the N type dopant in the surface layer 18 to diffuse completely into the SOI layer 16 to form an N+ buried layer 20. One example of an N+ buried layer formed in this manner is 2.5 microns thick containing Sb at a concentration of  $1.5 \times 10^{18}$  atoms/cm<sup>3</sup>, producing a 0.02  $\Omega$  cm layer.

There are alternative methods of controlling the doping level in the N+ buried layer 20. A first alternative is to form the non selective N+ SOI layer 16 directly by epitaxial growth without an N+ implant. In a second alternative, which is one preferred embodiment as depicted in FIG. 1a, the SOI layer 16 is initially lightly doped and a non selective N+ implant is then made into its surface. This method provides more precise control of the dose and location of the N+ dopant. It also allows use of commercially available bonded wafers as starting material. A third alternative is described below with reference to FIGs. 3a-3d. The common feature of these three versions is that the N+ buried layer is non selective across the entire wafer and is formed without a masking step.

Also shown in FIG. 1b is a mask 22 having an opening 24 through which P type dopants are implanted, as indicated by the arrows at the top of FIG. 1b, to form a surface layer 26 of P type dopants in opening 24. In one preferred embodiment boron is implanted at a dose level of  $1.5 \times 10^{15}$  atoms/cm<sup>2</sup> to form the surface layer 26.

In FIG. 1c mask 22 has been removed, and an N-epitaxial (epi) layer 28 has been grown onto the N+ buried layer 20. In one preferred embodiment N- epi layer 28 is grown to a thickness needed to support the desired breakdown voltage of the final integrated circuit transistor, for example 5 to 10 microns for a 30 volt device.

Fig. 1d depicts a further processed portion 10. After a mask 30 with an opening 32 has been applied to the N- epi layer 28, P type dopants are implanted, as indicated by the arrows at the top of FIG. 1d, to form a surface layer 34 of P type dopants in the opening 32.

FIG. 1e depicts the portion 10 after the mask 30 has been removed and a diffusion process performed which enlarges the N+ buried layer 20, forms a P+ buried layer 36 from the P type surface layer 26 and forms a P well 38 from the P type surface layer 34. The dashed line 40 indicates the original boundary between the N- epi layer 28 and the N+ buried layer 20. The dopant in the P+ buried layer 36 will over compensate the dopant in the N+ buried layer 20 in the region below the surface layer 26 of FIG. 1b leaving net P type down to the bond oxide 14.

Advantageously the dopant in P+ buried layer 36 is selected to have a higher diffusion coefficient than the N+ dopant in the N+ buried layer 20 so that the P+ buried layer 36 will out diffuse further into the overlaying N- epi layer 28 to connect with the P well 38 to form a P type buried layer at the bottom of the P well 38. If the dopant forming the N+ buried layer 20 had a higher diffusion coefficient than the dopant forming the P+ buried layer 36, the N+ buried layer 20 would extend above the P+ buried layer 36,

and the P well 38 would have to have a high enough dose concentration to over compensate the N+ buried layer 20 in order to make a connection with the P+ buried layer 36. If the P well 38 is the collector of a PNP transistor used, for example, for analog signal processing, then the N+ buried layer 20 would not be over compensated since the dopant concentration in the collector of such a transistor is several orders of magnitude less than the heavy doping generally used to form an N+ buried layer. While there are relatively slow and fast diffusing N type dopants, there is no slow diffusing P type dopant presently being used in silicon semiconductor manufacturing. Thus, with the dopants commonly used in semiconductor manufacturing, a non selective P+ buried layer cannot practically be used with a selective N+ buried layer in silicon.

FIG. 1f depicts the structure of FIG. 1d with the addition of a lateral isolation trench 42 thereby providing lateral as well as vertical dielectric isolation. The lateral isolation trench 42 may alternatively be formed before the process steps indicated in FIG. 1d.

In FIG. 1f the lateral isolation trench 42 is advantageously located contiguous to the P well 38 and the P+ buried layer 36 thus avoiding an isolated N+ buried layer region between the lateral isolation trench 42 and the P+ buried layer 36 which would result if the lateral isolation trench 42 were spaced apart from the P well 38 and the P+ buried layer 36.

As shown in FIGs. 1a-1f dual P+ and N+ buried layers (P+ buried layer 36 and N+ buried layer 20, respectively) have been formed wherein the N+ buried layer is non selective, formed across the wafer without requiring a mask

for the buried layer. In one preferred embodiment both buried layers have a sheet resistance of about 100  $\Omega$  per square.

As described above and shown in FIGs. 1a-1f, the P+ buried layer 36 is formed by an initial implant of P type dopants into a surface layer 26 but not diffused until after the N- epi layer 28 is grown and the P well 38 is formed by an initial implant of P type dopants into a surface layer 34. In an alternative process the P+ buried layer 36 is diffused down into the N- SOI layer 16 after being implanted but before the N- epi layer 28 is grown. In either case the total Dt (diffusion coefficient multiplied by diffusion time) experienced by the P+ region 26 is  $1.9 \times 10^{-8} \text{ cm}^2$  in one preferred embodiment, most of it to also down diffuse P well 36 in the case of this alternative process. Designs for other applications may require quite different Dt's as is well known in the art.

FIG. 2 depicts another alternative embodiment of the structure of FIG. 1e wherein the depth of P+ buried layer 36 does not reach all the way to the bond oxide 14. When a high enough implant dose of P type is used, the P+ buried layer 36 will diffuse down to the bond oxide layer 14 as shown in FIG. 1e, and over compensate the entire thickness of the N+ buried layer 20 leaving a net P type region everywhere in the regions implanted. However, if a lower P+ implant dose is used, a vestigial floating N+ region 48 will be left adjacent to bond oxide 14 under the P+ buried layer 36 as shown in FIG. 2. This is acceptable in cases where no connection is made to the N+ buried layer 20 and the P+ buried layer 36 is connected to the P well 38 as desired. Residual N+ region 48 may also occur with a thicker SOI



layer 16, a greater N+ buried layer doping or thickness, or a smaller Dt applied to the P+ buried layer, or combinations of these factors.

FIGs. 3a-3d depict an alternate method of forming the N+ buried layer 20 of FIG. 1b.

FIG. 3a depicts a portion 50 having an N+ device wafer 52 with a top oxide layer 54 and a bottom oxide layer 56. The top oxide layer 54 and bottom oxide layer 56 may be formed by oxidizing the N+ device wafer 52. In one preferred embodiment the N+ device wafer 52 is doped with a relatively slow diffusion coefficient dopant such as As or Sb. The doping level is selected at the level desired for the buried layer in the design, such as  $1.5 \times 10^{18}$  atoms/cm<sup>3</sup> as described above with respect to FIG. 1a.

FIG. 3b is FIG. 3a with a handle wafer 58 bonded to the bottom oxide 56.

FIG. 3c is FIG. 3b with the top oxide 54 and the top portion of the N+ device wafer 52 removed to provide an N+ SOI layer 60 which is also an N+ buried layer. Also, a P+ buried layer 62 has been formed in the top of the N+ SOI layer 60. The P+ buried layer 62 is formed by masking, implantation and diffusion in the manner described above with respect to FIGs. 1b and 1e.

FIG. 3d is FIG. 3c after the growth of an epi layer 64. The N+ SOI layer 60 up diffuses into the epi layer 64 and the resulting structure has an N- layer 66 on top of an N+ buried layer 68. The P+ buried layer 62 also up diffuses into the epi layer 64. The dotted line 72 indicates the top of the N+ SOI layer 60 and the bottom of the epi layer 64. The P well 38 shown in FIG. 1e can then be formed using masking, implantation and diffusion as described above.

This method of FIGs. 3a-3d eliminates the N<sup>+</sup> implant step and the following diffusion described above with respect to FIGs. 1a and 1b.

FIGs 4a-4i depict a dual N<sup>+</sup> and P<sup>+</sup> buried layer structure with a non selective N<sup>+</sup> buried layer utilizing vertical junction isolation and lateral dielectric isolation.

FIG. 4a depicts a portion 80 having a P<sup>-</sup> substrate 82 containing an N<sup>-</sup> isolation region 84. The N<sup>-</sup> isolation region 84 provides a conventional junction isolation and can be doped using, for example, phosphorus.

FIG. 4b is FIG. 4a after a further processing of portion 80 in which an N<sup>+</sup> surface layer 86 has been non selectively implanted, as depicted by the arrows at the top of FIG. 4b. The N<sup>+</sup> surface layer 86 is implanted using, for example, a slow diffusing dopant by any conventional method such as implant of arsenic.

FIG. 4c is FIG. 4b after a diffusion process which produces an N<sup>+</sup> buried layer 88 produced by the diffusion of the surface layer 86. In one preferred embodiment the majority N type dopant in the N<sup>+</sup> buried layer 88 is arsenic since it has a lower diffusion coefficient than phosphorus which is used to form the N<sup>-</sup> isolation region 84.

FIG. 4d depicts a further processing of portion 80 utilizing a mask 90 having an opening 92 through which P type dopants are implanted, as indicated by the arrows at the top of FIG. 4d, to form a surface layer 94 of P type dopants in the opening 92. In one preferred embodiment boron, which has a higher diffusion coefficient than arsenic used in the implantation of FIG. 4b, is selected for this P type implant.

In FIG. 4e a P+ buried layer 96, produced by the diffusion of the surface layer 94, has been formed within the N+ buried layer 88 and the N- isolation region 84.

In FIG. 4f an N- epi layer 98 has been grown on top of the structure of FIG 4e.

FIG. 4g depicts a further step in the processing in which a mask 100 is applied to the surface of the wafer with an openings 102 through which a surface layer 104 is formed by P type implantation as indicated by the arrows at the top of FIG. 4g. Again, in one preferred embodiment, boron is the dopant used to form the surface layer 104.

FIG. 4h depicts the structure of FIG. 4g after the mask 100 has been removed and another diffusion operation performed. As shown in FIG. 4h the diffusion of the surface layer 104 produces a P well 106 which has diffused down to intersect the up diffused P+ buried layer 96. The P well 106 can form the collector of a PNP transistor (not shown in the drawings).

As shown in FIG. 4h the P+ buried layer 96 up diffuses further than the N+ buried layer 88 because it is made with a dopant that has a higher diffusion coefficient than the dopant used to form the N+ buried layer 88 and has been subjected to a sufficiently large Dt. The P+ buried layer 96 implant dose may be chosen high enough that it over compensates the N+ buried layer 88 throughout its entire thickness. An alternative structure, similar to that described above with respect to FIG. 2, may arise in which a region of net N, corresponding to region 48 of FIG. 2, connected at its ends to the N- isolation region is left in the middle of the P+ buried layer. This alternative

structure results from alternative processing as described above with reference to FIG. 2.

In FIG. 4i three lateral isolation trenches 108 have been etched from the surface of portion 80 down into the P-substrate 82 below the depth of the N- isolation region 84. Channel stop implants 110 were made into the bottoms of the lateral isolation trenches 108, and isolation dielectric layers 112 were formed on the sides of the lateral isolation trenches 108 which were then filled with polysilicon 114. These isolation trenches can also be formed before the process indicated in FIG. 4g.

In FIG. 4j an N+ contact 116 to the N- epi layer 98 and near the P well 106 has been formed in the surface to provide an ohmic contact to the N- epi layer 98. The N+ contact 116 is typically formed by a step used to form some other device region such as emitter and collector contacts for NPN devices. The N+ contact 116 connects to the N- isolation region 84 through the continuous path of N type material comprising the N- epi layer 98 and the N+ buried layer 88 to provide an ohmic connection between a surface conductor (not shown) contacting the N+ buried layer 88 and the N- isolation region 84. The surface conductor might, for example, connect the N+ contact 116 to the P well 106 that might be the collector of a PNP transistor. The N+ contact 116 can also be used, if desired, in a fully dielectrically isolated structure such as shown in FIG. 1f.

FIG. 4j, in contrast to FIG. 1f, depicts the lateral isolation trenches 108 on either side of the P well 106 as spaced apart from the P well 106 and the P+ buried layer 96. At least one of these isolation trenches 108 must be spaced apart to allow room for an N+ contact to provide an N type

electrical path to the N- isolation layer 84. Since the N- isolation layer 84 meets the N+ buried layer 88 on both sides of the P+ buried layer 96 thereby forming an electrical connection to the two N+ buried layer regions, both of the lateral isolation trenches 108 may be spaced apart from the P well 106 and the P+ buried layer 96.

FIG. 4k is FIG. 4j with the addition of an NPN transistor and a PNP transistor including the respective collector contacts, bases and base contacts, and emitters.

As shown in FIGs. 4a-4k dual P+ and N+ buried layers (P+ buried layer 96 and N+ buried layer 88, respectively) have been formed wherein the N+ buried layer is non selective, formed across the wafer without requiring a mask for the buried layer.

FIGs. 5a-5g, 6a-6e and 7a-7c depict a dual N and P buried layer structure with a non selective N buried layer in which the buried layers are formed in a surface of the device wafer that becomes the bottom of the final device island. More particularly, FIGs. 5a-5g and 6a-6e depict a bonded wafer structure, and FIGs. 7a-7c depict a single poly dielectric isolation structure.

FIG. 5a depicts a portion 120 having an N- substrate 122 containing a P collector 124. The structure of FIG. 5a may be formed by, for example, starting with an N- wafer and then implanting and diffusing boron to form the back diffused P collector 124.

FIG. 5b depicts a further processing of portion 120 of FIG. 5a in which an N+ surface layer 126 has been non selectively implanted, as depicted by the arrows at the top of FIG. 5b. The N+ surface layer 126 is implanted using, for example, a slow diffusing dopant by any conventional

method such as implant of arsenic. The N+ layer 106 can alternatively be formed by epitaxial deposition on the surface of the substrate 122 after deposition of the P collector 124.

FIG. 5c is FIG. 5b after a diffusion process producing an N+ buried layer 128 by the diffusion of the surface layer 126.

FIG. 5d depicts a further processing of portion 120 utilizing a mask 130 having an opening 132 through which P type dopants are implanted, as indicated by the arrows at the top of FIG. 5d, to form a surface layer 134 of P type dopants in opening 132. In one preferred embodiment, the P type dopant is boron, which has a faster diffusion coefficient than the N type dopant, arsenic, used in this preferred embodiment for the implantation of FIG. 5b.

FIG. 5e is an optional process step before an epi layer is grown as depicted below in FIG. 5f. In this optional step the surface layer 134 is partially diffused to form a P+ buried layer 136. Either the entire diffusion or the completion of this partial diffusion shown in FIG. 5e is done sometime after the structure of FIG. 5g has been formed by the further processing of the wafer (not shown in the drawings).

In FIG. 5f the device wafer of FIGs. 5a-5e is bonded to a handle wafer 138 with an insulator, shown as buried oxide 140, between them. Also, the bottom 142 of the device wafer is thinned to the desired thickness for device islands in the process and also intersecting the P collector diffusion so that the P collector 124 extends through the entire thickness of the final device wafer.

In FIG. 5g the portion 120 of FIG. 5f has been inverted and lateral isolation trenches, as indicated by lateral isolation trench 144, have been formed to extend down to the buried oxide 140.

In the above description the non selective N+ buried layer is formed before the selective P+ buried layer. The selective layer may be formed before the non selective layer as shown in FIGs. 6a-6e.

FIG. 6a is a redrawing of FIG. 5a for convenience.

FIG. 6b depicts the mask 130 with an opening 132 and implanted to form the P+ surface region 134 as described above relative to FIG. 5d.

FIG. 6c is FIG. 6b after the P+ surface region 134 has been diffused to form the P+ buried layer 136.

FIG. 6d depicts the non selective implantation of the N+ surface region 126 as described above relative to FIG. 5b.

FIG. 6e is FIG. 6d after a diffusion operation with the N+ buried layer 128 formed after the diffusion. FIG. 6e is the same as FIG. 5e.

FIGs. 7a-7c depict a single poly dielectric isolation structure.

In FIG. 7a the portion 120 of FIG. 5e has been moat etched using a masked silicon etch to define a series of mesa shaped structures 146 which will become device islands completely separated by dielectric isolation as shown in the following FIGs. 7b and 7c.

In FIG. 7b the exposed top and side surfaces of the portion 120 have been oxidized to form as oxide 148, and polysilicon, shown as poly 150, has been deposited to fill the moats and build up a support thickness on the wafer.

In FIG. 7c the wafer has been thinned, as shown by bottom edge 152, to the thickness desired for islands 146 in which devices will be formed. In this process the moats of poly 150 are intersected to complete the formation of isolated islands 146, and the P collector 124 is intersected so that it extends through the entire thickness of the final device island 146.

Although the invention has been described in part by making detailed reference to a certain specific embodiment, such detail is intended to be, and will be understood to be, instructional rather than restrictive. It will be appreciated by those skilled in the art that many variations may be made on the structure and mode of operation without departing from the spirit and scope of the invention as disclosed in the teachings contained herein.